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10/632,431	07/31/2003	Hong Wang	42P15449	2852

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,431	WANG ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-29,32 and 34-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15,17-23,25-29,32 and 34-37* is/are rejected.

7)☒ Claim(s) *14 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4 and 5 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The use of "the control logic" qualified with the functionality of the logic to describe multiple logics is extremely confusing. Additionally, both claims lack antecedent basis for the second instance of control logic. Examiner suggests changing each instance of control logic to "a first control logic", "a second control logic", etc… This problem is compounded in claims such as claim 6 where “the control logic” is used alone to reference control logic.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-13,15,17-23,25-29,32 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg et al. (Slipstream Execution Mode for CMP-Based Multiprocessors) herein referred to as Rotenberg, in view Brown et al. (Speculative Precomputation on Chip Multiprocessors) herein referred to as Brown.

5. *Note that the Brown reference is written by a different inventive entity than the current application and is therefore eligible as prior art under 35 USC 102(a): See MPEP Section 2132 subsection III regarding "by others".*

6. Referring to claim 1, Rotenberg discloses an apparatus comprising: a first processor (Such as Processor 0, see Figure 2) to execute a main thread instruction stream (Task 0 (R)) that includes a delinquent instruction (any load which misses in the R-stream), wherein the first processor is to be associated with a first private cache (L1 data cache of that processor; see first paragraph of section 2); a second processor (Such as Processor 1; see Figure 2) to execute a helper thread instruction stream (A-Stream) that includes a subset of the main thread instruction stream (See section 3.2, second paragraph), wherein the subset includes the delinquent instruction (Any program will inherently include cache misses), wherein the second processor is to be associated with a second private data cache (L1 data cache of that processor; see first paragraph of section 2); wherein said first and second processors each include a private data cache (L1 data Cache, see section 2, first paragraph); a shared memory system (Unified L2 cache; see section 2, first paragraph) coupled to said first processor and to said second processor; and logic to retrieve, responsive to a miss of requested data (any data not in L1 cache) for the delinquent instruction (instruction referencing data not

in cache) in the private cache of the second processor (lines which are not referenced at all by the A-Stream, see 2nd last paragraph of section 3.4), the requested data from the shared memory system (see see 2nd last paragraph of section 3.4); the logic further to provide requested data to the first processor (see the first paragraph of section 3 regarding preloading shared data into the L2 cache).

Rotenberg does not expressly disclose control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache associated with the second processor, the requested data to the first private cache associated with the first processor.

Brown teaches control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache associated with the second processor, the requested data to the first private cache associated with the first processor (See section 5.1, Figure 3(b)).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Rotenberg by pushing data into the private cache of the first processor responsive to a miss as taught by Brown in order to "effectively reduce the miss rates of the private caches, thereby improving the timeliness of prefetches." (Brown, first paragraph of page 6).

7. Regarding claim 2, Rotenberg also discloses the first processor, second processor and logic are included within a chip package (see abstract), and wherein the

shared memory system includes a shared cache (L2 cache, see first paragraph of section 2).

Regarding claim 3, Rotenberg also discloses retrieval logic coupled to the control logic to retrieve the requested data from the shared memory system in response to the miss of the requested data for the delinquent instruction in the second private cache (Inherently, if the data misses in the L1 cache, it must be requested from the L2 [or higher level memory]; see first paragraph of section 2).

8. Regarding claim 4, Rotenberg does not expressly discloses the control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to broadcast the requested data to an affinity group of processors including at least the first processor.

Brown teaches control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to broadcast the requested data to an affinity group of processors including at least the first processor (see Section 5.1; Figure 3(b)).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have combined the inventions of Rotenberg and Brown as shown above regarding claim 1.

9. Regarding claim 5, Rotenberg does not expressly discloses the control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to unicast the requested data to the first processor.

Brown teaches control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to unicast the requested data to the first processor (see Section 5.1; Figure 3(a)).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have combined the inventions of Rotenberg and Brown as shown above regarding claim 1.

10. Claim 6 recites limitations equivalent to those discussed above regarding claim 1.

11. Claim 7 recites equivalent limitations as claim 1 with the following exceptions which are taught by Rotenberg. The claim is rejected for the same reasons stated above.

Rotenberg discloses the second thread including a load instruction from the first thread that a miss to the first private cache is anticipated (see the last two paragraphs of the left column of page 2 regarding prefetching instructions in order to decrease latency)

12. Claims 8 and 9 recite equivalent limitations as claims 4 and 5 and are rejected for the same reason.

13. Regarding claim 10, Rotenberg does not expressly disclose the higher level memory includes a memory coupled external to the processor, and wherein the first processor core is further to trigger the second processor core's execution of the second speculative thread responsive to execution of a trigger instruction in the first thread with the first processor core.

Brown teaches the higher level memory includes a memory coupled external to the processor (See fig. 1(b)), and wherein the first processor core is further to trigger the second processor core's execution of the second speculative thread responsive to execution of a trigger instruction in the first thread with the first processor core (see the first paragraph of the right column of page 1).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Rotenberg by triggering the second

processor core responsive to a rigger instruction in the first thread as taught by Brown in order to "effectively reduce the miss rates of the private caches, thereby improving the timeliness of prefetches." (Brown, first paragraph of page 6).

14. Claim 11 recites equivalent limitations as set forth in claim in claim 1 and is therefore rejected using the same grounds as claim 1.

15. Regarding claim 12, Rotenberg also discloses a third processor (See Figure 2 regarding the multitude or processors) and a shared memory system coupled to said first processor and to said second processor (see the first paragraph of section 2), and said third processor.

16. Regarding claim 13, Rotenberg does not expressly disclose retrieval logic to retrieve, responsive to a miss of requested data for the delinquent load instruction in the second data cache, the requested data comprises: the retrieval logic, responsive to the miss of requested data for the delinquent load instruction in the second data cache, to issue a snoop for the requested data to a third data cache associated with the third processor, and the third data cache to provide the requested data to the retrieval logic in response to receiving the snoop issued from the retrieval logic.

Brown teaches retrieval logic to retrieve, responsive to a miss of requested data for the delinquent load instruction in the second data cache, the requested data comprises: the retrieval logic, responsive to the miss of requested data for the

delinquent load instruction in the second data cache, to issue a snoop for the requested data to a third data cache associated with the third processor, and the third data cache to provide the requested data to the retrieval logic in response to receiving the snoop issued from the retrieval logic (See section 5.2).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have combined the inventions of Rotenberg and Brown as shown above regarding claim 1.

17. Claim 15 recites equivalent limitations as claim 2 and is rejected under the same grounds.

18. Claim 17 recites equivalent limitations as claim 10 and is rejected for the same reasons.

19. Claims 18 and 25 recite equivalent limitations as claims 1 and is rejected for the same reasons.

20. Claim 19 recites limitations already discussed above regarding claim 4 and is rejected for the same reasons.

21. Claim 20 recites limitations already discussed above regarding claims 1 and 6 and is rejected for the same reasons.

22. Claim 21 recites limitations already discussed above regarding claims 1 and 4 and is rejected for the same reasons.

23. Claim 22 recites limitations already discussed above regarding claim 13 and is rejected for the same reasons.

24. Claim 23 recites limitations already discussed above regarding claim 4 and is rejected for the same reasons.

25. Claim 25 recites limitations already discussed above regarding claim 1 and is rejected for the same reasons.

26. Claim 26 recites limitations already discussed above regarding claim 4 and is rejected for the same reasons.

27. Claim 27 recites limitations already discussed above regarding claim 1 and is rejected for the same reasons.

28. Claim 28 recites limitations already discussed above regarding claim 3 and is rejected for the same reasons.

29. Claim 29 recites limitations already discussed above regarding claim 13 and is rejected for the same reasons.

30. Claims 32-37 recites limitations already discussed above and are rejected for the same reasons.

Allowable Subject Matter

31. Claims 14 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

Jesse R Moll
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/J. R. M./

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